ADVANCED PROCESSOR PLATFORMS FOR DEVICES

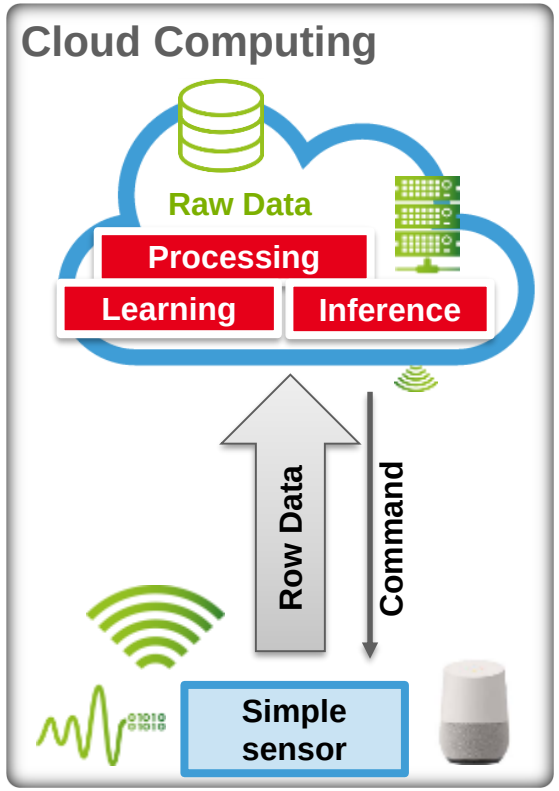
Carlo Reita

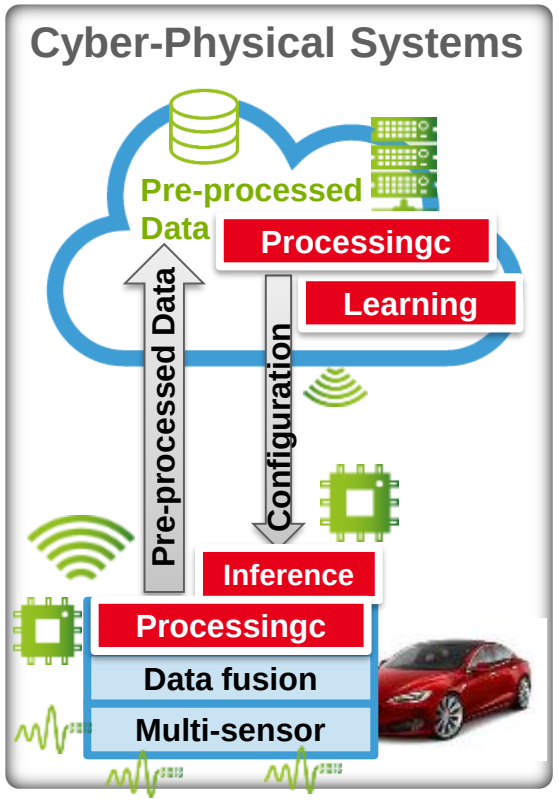
Stakeholder Workshop – Smart Networks and Services Partnership, 2 October 2019, Dresden

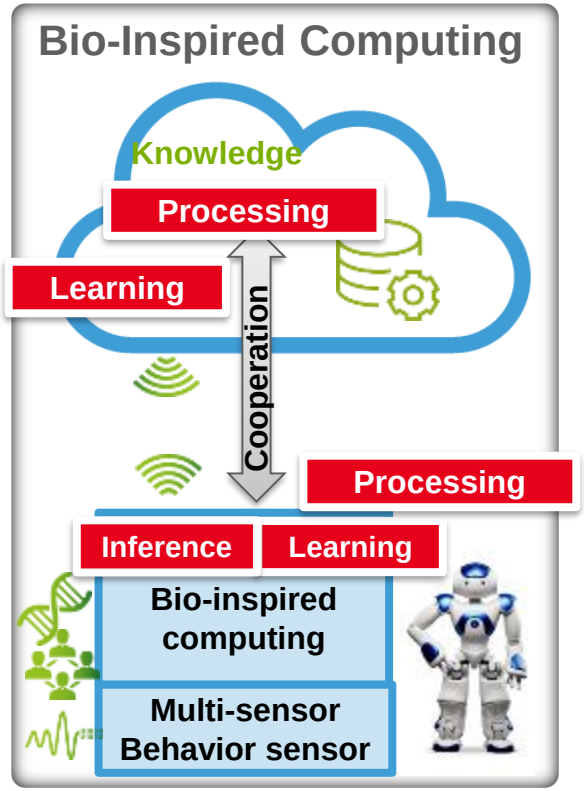
CONTEXT

- Evolution of Networks and usages will require more computing all along the communication chain
- Sovereignty and benefits to the citizens at large can be guaranteed only by EU actors strong presence at all levels of the supply and value chains
- New networks and applications can represent the return of EU industry to consumer and infrastructure industry

Network distributed computing need specialized hardware







- Optimize power consumption
- Reduce data transfer
- Reduce latency
- Integrate sensing and processing

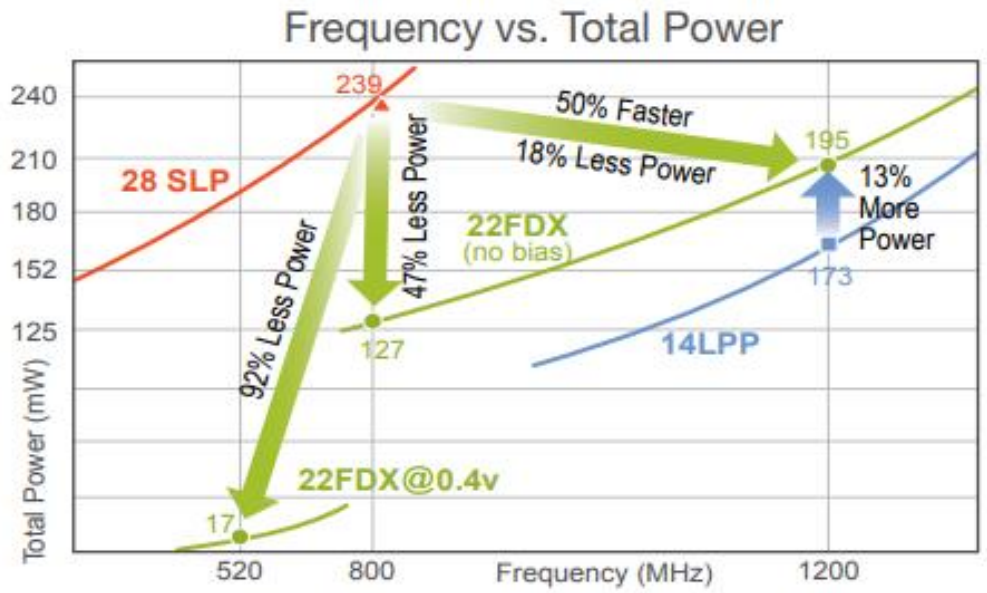
- Adaptation to the environment, customization
- Incremental / Online learning
- Design and Programming Software tools

1

Technology

FDSOI EU Leading Technology

High Performance and Low Power



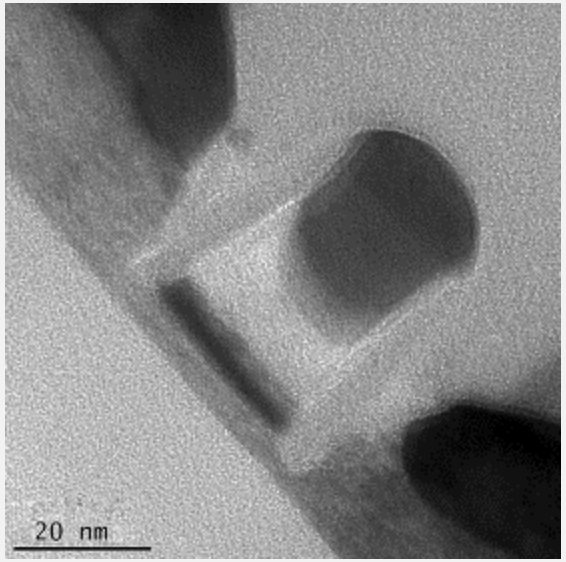
GLOBALFOUNDRIES

IP Overview

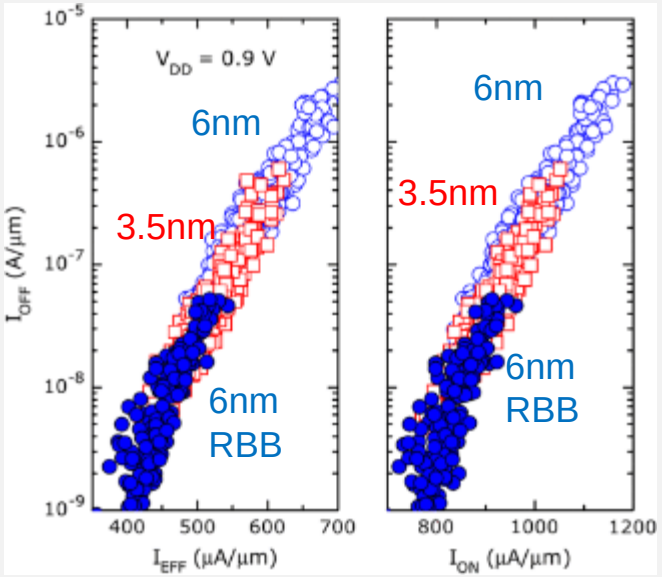
The 22FDX Platform IP portfolio includes a wide range of silicon-proven high performance, power-optimized solutions for a broad set of applications.

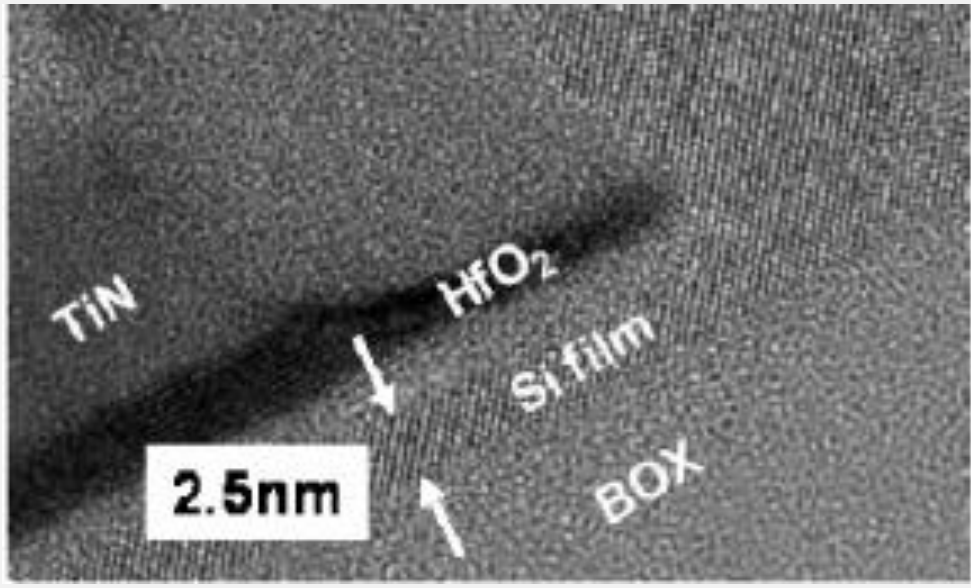
Foundation IP					
Standard Cell	Low Power/Performance/Dense/Low Leakage Libraries				
Memory	HP/HD/ULL/TP/DP, SRAM, Register File, ROM				
GPIO	1.2-1.8V/3.3V, ESD				
Body Bias	Body Bias Generator, Dynamic Body-bias Controller				
Interface IP					
DDR3/4	LPDDR3/4	USB2/3.x	PCIe	SATA	
SERDES	MIPI D-PHY/ M-PHY	HDMI 2.0	LVDS	XAUI	
Wireless Connectivity IP				**Non-volatile Memory IP**	
BLE	WiFi	NB-IoT	Cat-M1	OTP	eFuse
Analog IP					**Core IP**
PLL	ADC/ DAC	Video DAC	Audio CODEC	LS	RISC-V
RTC	Temp Sensor	Process Monitor	POR/ BOR	Regulator	

FDSOI device scalability: experiments



A. Khakifirooz et al., EDL'12 (IBM)

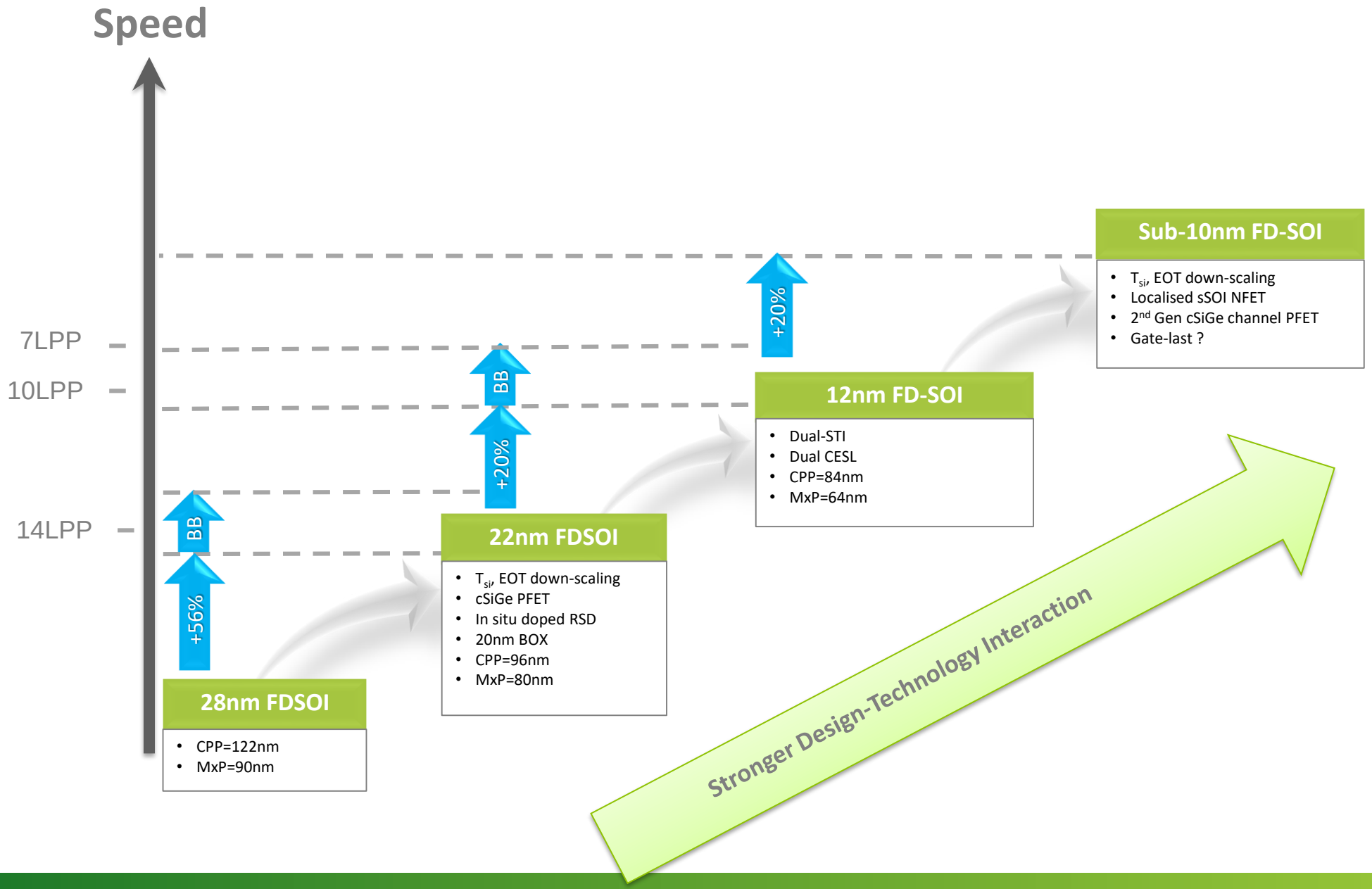




See also K. Uchida works with poly/SiO2 gate stacks

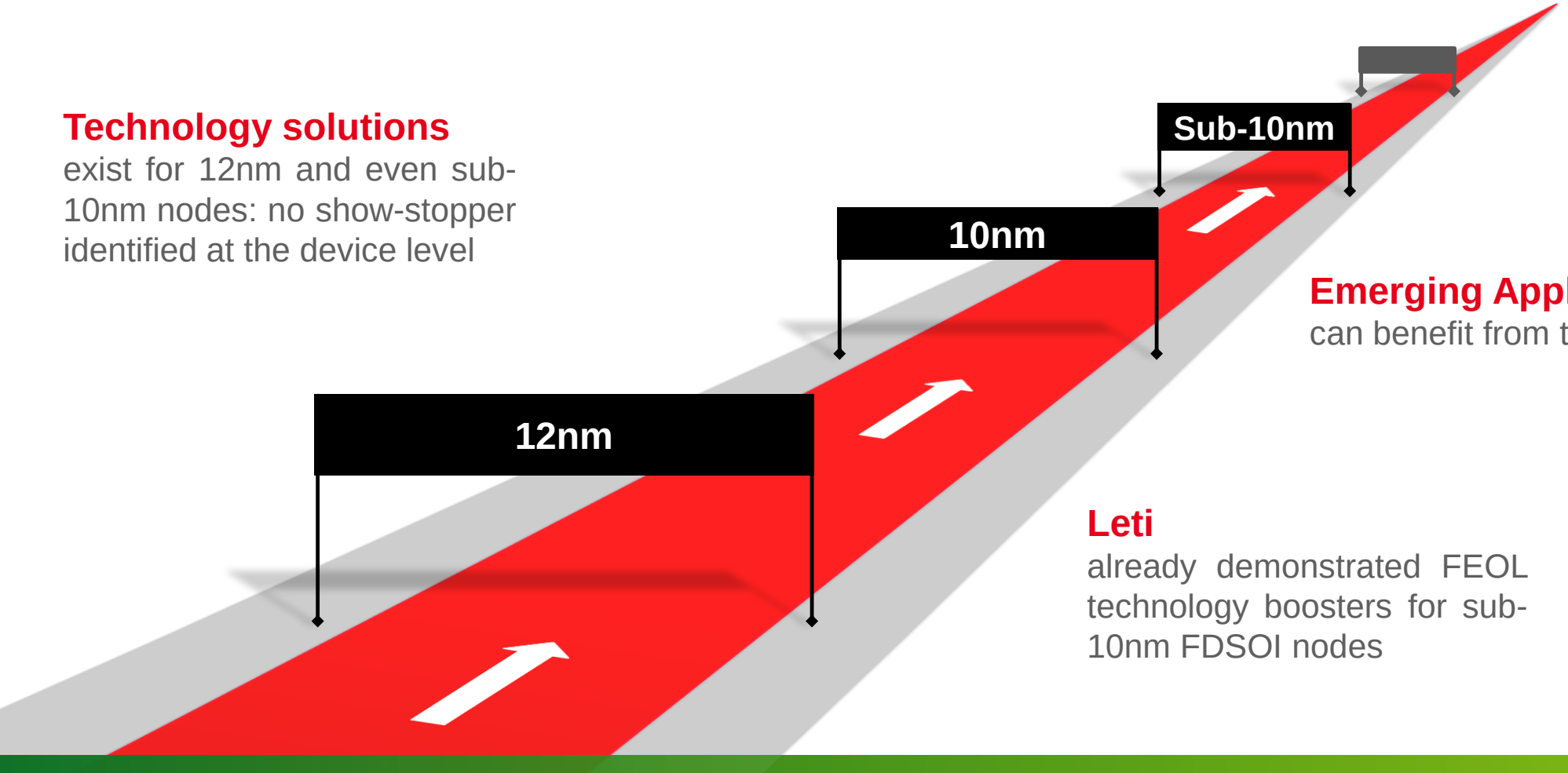
- Extremely scaled FDSOI CMOS have already demonstrated
- With excellent device performance

FDSOI Roadmap



A roadmap for power efficiency and performance in Europe

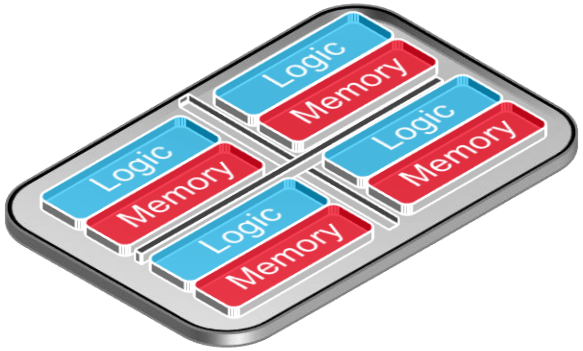
Technology solutions
exist for 12nm and even sub-10nm nodes: no show-stopper identified at the device level



Emerging Applications (AI, 5G,…)
can benefit from this FDSOI technologies

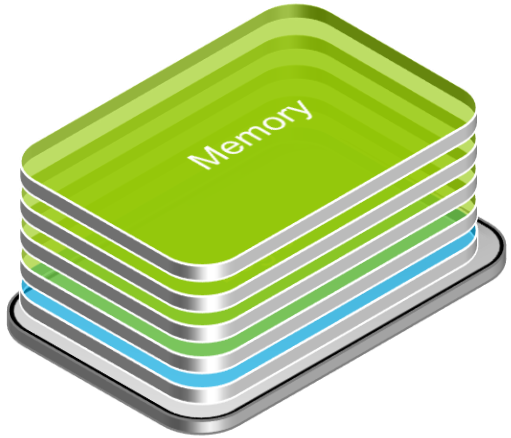
Leti
already demonstrated FEOL technology boosters for sub-10nm FDSOI nodes

And then going up

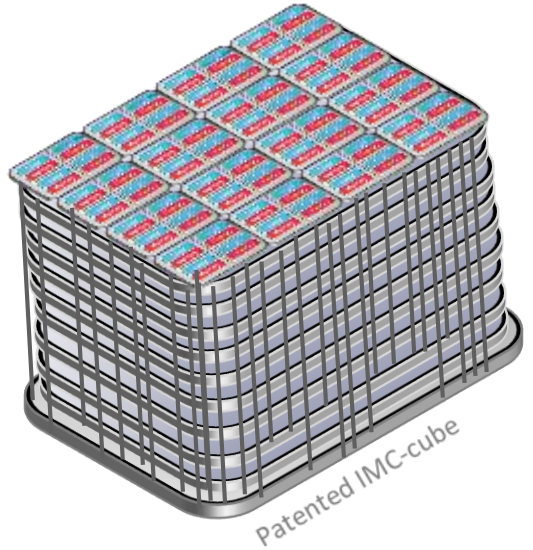


In memory computing

Logic Stacking



Memory Stacking



In Memory Computing Stacking

2

Ecosystem

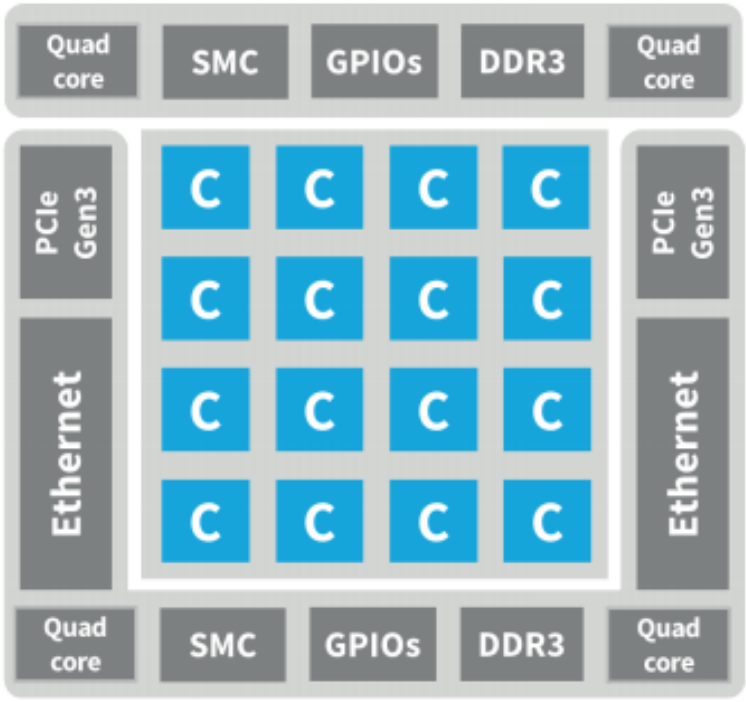
Industrial environment in EU

- ***Europe has lost his position in advanced digital design and fabrication***

- **But this is not irreversible:**

  - Important competences are still present
  - Market and applications evolution (like 5G and 6G) open up new opportunities
  - EU citizens demands, regulations and sovereignty need specific EU solutions

Kalray: High performance multicore



MPPA® Bostan with 16 clusters

Core architecture

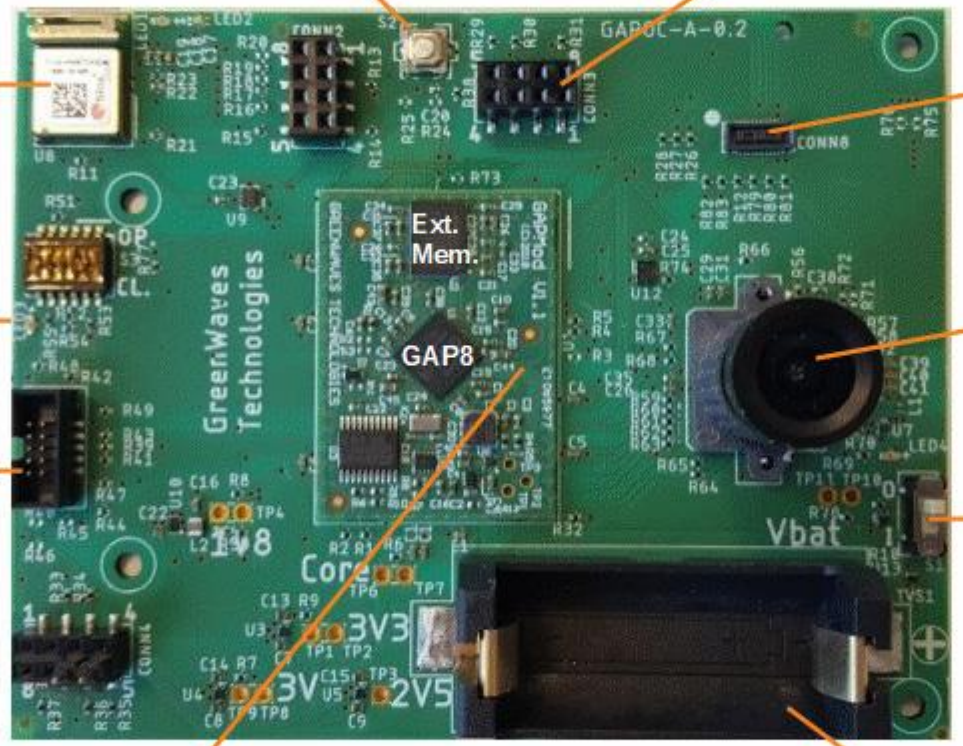
Compute/System Cores

- 64-bit/32-bit architecture / 600Mhz
- 5-issue VLIW cores
- 8KB instruction cache / 8KB data cache
- IEEE 754-2008 Floating Point Unit (FPU)
- 1 FLOPs (SP) / 0.5 TFLOPs (DP) / 1 TOPs
- Memory Management Unit (MMU)
- ISA with extensions for encryption
- Crypto co-processors (AES, SHA, CRC, etc.)

Master cores

- 64-bit/32-bit architecture
- 32KB instruction cache per core
- 32KB data cache shared between 4 cores
- Data cache can be configured as a shared 128KB data cache among 4 SMP Quad cores
- Memory Management Unit (MMU)

Greenwaves: Computer Vision Battery Powered



Connectors (x3):
2.54mm pitch, 0.5mm height, top+bottom entry
Access to various GAP8 GPIOs & interfaces

Reset Button

BLE Module w/
integrated antenna

Green LED,
s/w controllable

10-pin JTAG header

Ultra low profile Hirose DF40 connector
For optional « clip on » satellite board

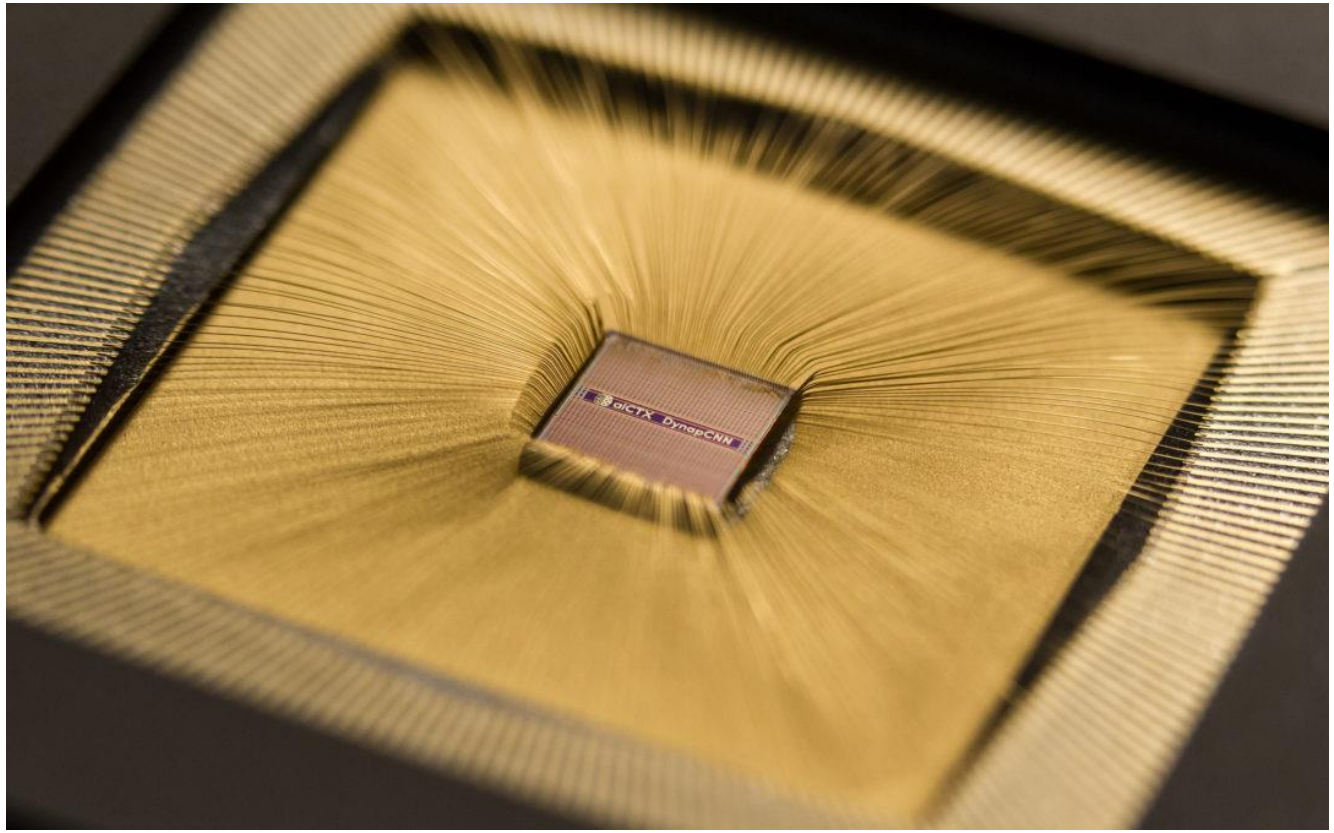
Image sensor
with interchangeable M12 lens on S-mount
(up to WVGA, HDR, Monochrome)

Global power On/Off switch

GAPMod Core Module
Includes GAP8 + Cypress HyperRAM-HyperFlash MCM (64Mbit+512Mbit)

Holder for 2/3A battery (3.6V)

aiCTX: World's First 1M Neuron, Event-Driven Neuromorphic AI Processor for Vision Processing



- **DYNAP-CNN** is a 12mm2 chip, fabricated in **22nm FDSOI** technology, housing over 1 million spiking neurons and 4 million programmable parameters, with a scalable architecture optimally suited for implementing Convolutional Neural Networks..

- Issued from the H2020 program NeuRAM3

- Higher energy efficiency at same performance than Intel Loihi

Industrial environment in EU

- *Europe has lost his position in advanced digital design and fabrication*

- **But this is not irreversible:**

  - Support is needed for both the design and technology communities to maintain an healthy ecosystem

  - IDMs, foundries and fabless have all a role to play.

Submissions /Acceptance EU

	Submitted	Accepted	% of total
2015	132	49	24
2016	120	48	23
2017	139	39	19
2018	109	35	17
2019	85	30	15

- EU dropped another 22% in 2019
  (21% drop in 2018)!
- NA & FE increased 3-5%
  (0-1 % in 2018)

- Digital Systems (4.6%)
- Power Management (8%)

- Europe Research Centers & Universities are suffering (50% reduction last year)
- Need some support to be at the top level

5G Funded projects

Since 2015, H2020 has been actively investing in the development and the roll-out of 5G. The European Commission invested over **700MEUR** in 5G PPP projects over 3 different phases:

- H2020 Phase 1 (2015): funding projects focusing on performing fundamental research for 5G networks
  - => 19 projects
- H2020 Phase 2 (2017): funding projects focusing on proof-of-concepts, experiments, verticals.
  - => 21 projects
- H2020 Phase 3 (2018): funding projects on the rollout of a 5G platform and large-scale & cross-boarder end-to-end trials
  - => 16 projects

- ***Only few projects integrate circuit design activities and none of them Components development***
- ***Phase 3 demonstrator rely on COTS or dedicated products from US & ASIA***

Why HE should improve on H2020 for Platform Components Development ?

- Demonstrator with COTS are lower **cost**, need less **resources** is less **risky** and can be more **powerful** than silicon demonstrator

- As a conclusion, a project proposal with COTS demonstrator will be far more competitive than a proposal with Silicon based demonstrator

- However, COTS demonstrators **DO NOT DEMONSTRATE** the suitability of the approach for consumer products
- COTS demonstrators **DO NOT POSITION** Europe for the future markets, no added value
- New European Fabless companies should emerge

Why HE should improve on H2020 Components Development ?

- Demonstrator with COTS are lower **cost**, need less **resources** is less **risky** and can be more **powerful** than silicon demonstrator

- **Dedicated EU Calls are needed to support Innovative Component Design, Fabrication and Test from R&D groups and Design Houses to stimulate the emergence of new actors**

- **Dedicated schemes to support fabrication of demonstrators in EU are needed to insure access to domestic technologies for the above groups**

Industrial environment in EU

Boosting Electronics Value Chains in Europe

A report to Commissioner Gabriel

19 June 2018

SOITEC, STMicroelectronics, X-FAB, Robert Bosch, ASML, Globalfoundries, UMS, Infineon, FhG uEV, CEA-LETI, imec

7. Seizing new opportunities

New computing paradigms, such as neuromorphic/quantum computing accelerators and complex integration, present new opportunities for developing the next generation of distributed/edge computing as well as centralised computing for the cloud (HPC) supporting the digital transformation of Europe. ***Europe must, therefore, take a leadership role in the development of these technologies.***

8 **Create a pan-European research infrastructure for advanced computing technologies**

We are calling for the creation of a pan-European infrastructure for developing, testing, experimenting and innovating in advanced computing technologies, leading to delivery of a digital hardware computing toolbox for European industries. A "moon-shot", mission-driven approach will be needed to achieve this European next-generation computing platform exploiting ultra-low power technologies and neuromorphic/quantum accelerators. This will require:

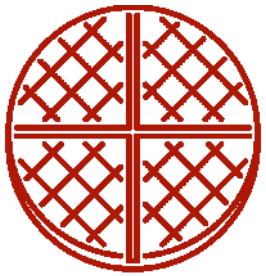
- the set-up of a joint state-of-the-art technological platform at European RTOs to design, manufacture and test prototype devices of future-generation processors and accelerators in order to prepare for an industrial uptake of these new technologies in European systems houses;
- the commitment of leading European micro-/nanoelectronics RTOs to forge a strategic alliance in close alignment with European semiconductor manufacturers, IDMs and foundries, as well as system houses to reach this goal.

EU RTOs cooperation for Next Generation Computing (NGC alliance)

imec leti cea tech Forschungsfabrik Mikroelektronik Deutschland

NGC Alliance : key indicators (3 RTOs combined)

9.000
researchers



35.000 m²
cleanroom

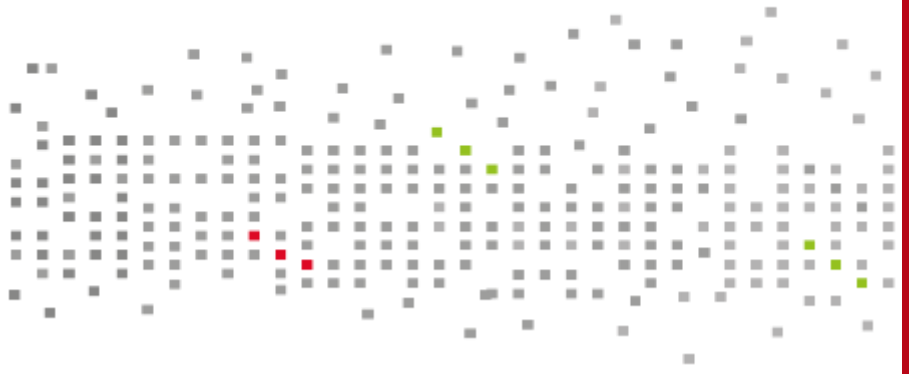
€1.300 million
annual budget

180 startups
created

3.000 publications
each year

7.000 patents
in portfolio

Join our ambition !



Leti, technology research institute
Commissariat à l'énergie atomique et aux énergies alternatives
Minatec Campus | 17 rue des Martyrs | 38054 Grenoble Cedex | France
www.leti-cea.com